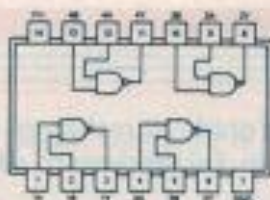


Quadruple
2 - input
positive
NAND gates
00



Quadruple
2 - input
positive - NOR
gates
02

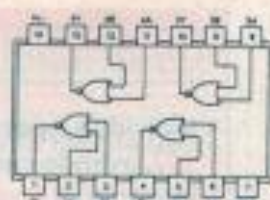
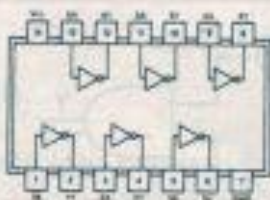


Fig. 106
Piedinature di
alcuni circuiti
integrati SSI della
serie digitale 74
(tensione di
alimentazione
 $+5\text{ V} \pm 5\%$).

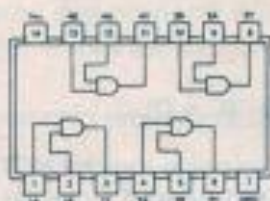
Hex inverters
04



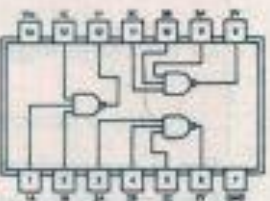
Quadruple
2 - input
positive
AND gates
08



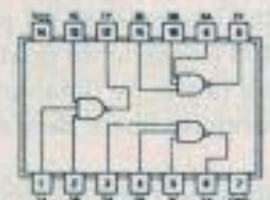
Quadruple
2 - input positive
AND gates with
open collector
outputs
09



Triple
3 - input
positive
NAND gates
10



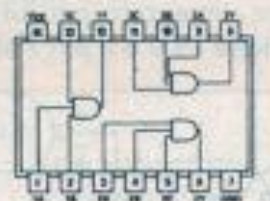
Triple 3 - input
positive NAND
gates with open-
collector outputs
12



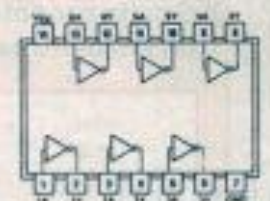
Hex
Schmitt-Trigger
inverters
14



Triple 3 - input
positive AND gates
with open-collector
outputs
15



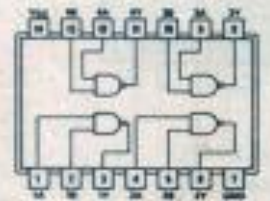
Hex inverter
buffers/drivers
with open collector
high-voltage
output
16



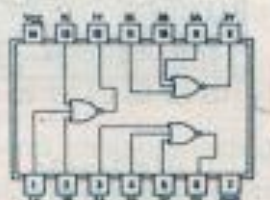
Hex buffers /
drivers with open-
collector high-
voltage outputs
17



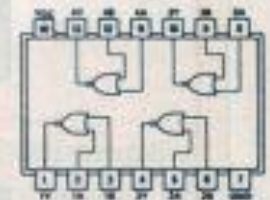
Quadruple
2 - input
high-voltage
positive - NAND
gates
26



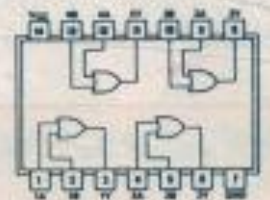
Triple
3 - input
positive - NOR
gates
27



Quadruple
2 - input
positive - NOR
buffers
28



Quadruple
2 - input
positive - OR
gates
32



Quadruple
2 - input
exclusive - OR
gates
86

